IN THE SPECIFICATION

Please replace the paragraph beginning at line 13, page 6 and ending at line 9, page 7 with the following rewritten paragraph:

Figure 4 illustrates a preferred embodiment of a Receive Data Path which strips the LARQ header to support frame priority in accordance with the present invention. The Receive Data Path 202 comprises a PM_RXDEC logic block 402, a PM_RXFCON logic block 404, a PM_RXNIB logic block 406, and a ~~PM_PXFCSGE~~ PM_RXFCSGEN logic block 408. When a frame with a LARQ and a Q Tag is received, the registers in the Registers and MIB Counters 216 asserts a signal, strip_LARQ, to the PM_RXDEC 402 to indicate that the LARQ is enabled so it must be stripped from the frame with the Q Tag, via step 302. The PM_RXDEC 402 then asserts the rm_sfcs signal and the rm_slarq signal to the PM_RXFCON 404. The asserted rm_sfcs signal indicates that the FCS in the frame with the Q Tag is to be stripped. The asserted rm_slarq signal indicates that the LARQ in the frame with the Q Tag is to be stripped. The PM_RXFCON 404 then strips the FCS and the LARQ, via step 304. Next, the PM_RXFCON 404 asserts a rb_str_larq signal to the PM_RXNIB 406. The asserted rb_str_larq signal indicates that the LARQ has been stripped from the frame with the Q Tag. The PM_RXNIB 406 generates the frame control frame accordingly. The PM_RXNIB 406 asserts an enfcs signal to the PM_RXFCSGEN 408. The asserted enfcs signal enables FCS recalculation for the stripped frame with the Q Tag. The PM_RXFCSGEN 408 then recalculates the FCS for the stripped frame with the Q Tag, via step 306. The recalculated FCS is added to the stripped frame with the Q Tag, and this frame is sent to the Ethernet controller 112, via step 308.